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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,111	12/30/2003	Richard Willson Arnold	TI-36471	3162

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,111	ARNOLD ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *13-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/30/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of claims 1-12 and 17-20 in the reply filed on 14 Mar. 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Specification

2. Claim 17 objected to because of the following informalities: the word 'ship' in line 5 should read 'chip'. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 3 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 3, recited the limitation "the conductive liner" in line 1. There is insufficient antecedent basis for this limitation in the claim.

For the purpose of examination, assuming claim 3 depends on claim 2.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-6 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5130768 to Wu et al.

Regarding claim 1, Wu discloses a semiconductor chip package in fig. 4 comprising: an integrated circuit chip 40, column 3 line 65, a chip contact pad 44, column 5 line 21, formed on a first side of the chip; a stud 80, column 5 line 40, formed on the chip contact pad 44, the stud being formed from wire using a wire bonding machine, column 9 lines 5-10, the stud 80 having an elongated portion extending from the chip contact pad 44; a substrate 12, column 4 line 15, comprising a first layer 59 of insulating material, column 8 line 14, on a first side of the substrate 12, a well 15, column 8 line 14, formed in the first layer 59 (159 in fig. 3) and opening to the first side of the substrate 12, the well having a bottom, a first conductive material (solder 15), column 8 line 12, that at least partially fills the well 15, and a second layer 158, fig. 3, column 7 line 23, having conductive trace lines 154, column 7 line 18, formed therein, wherein the first conductive material (solder 15) is electrically connected to at least one of the trace lines 154, fig. 4, and wherein the stud 80 is partially embedded in the first conductive material (solder) to form an electrical connection between the chip 40 and

the substrate 12, and wherein the first side of the chip faces the first side of the substrate, fig. 4.

Regarding claim 2, Wu discloses the semiconductor chip package of claim 1, further comprising: a conductive liner 56, column 8 line 15, at least partially lining the well 15, wherein the first conductive material (solder) in the well 15 is electrically connected to the at least one trace line 154 via the conductive liner 56.

Regarding claim 3, Wu discloses the semiconductor chip package of claim 2, wherein the conductive liner 56 comprises copper, column 7 line 22.

Regarding claim 4, Wu discloses the semiconductor chip package of claim 1, wherein the stud 80 comprises gold, wherein the outermost surface of the contact pad 44 comprises gold, column 9 line 7.

Regarding claim 5, Wu discloses the semiconductor chip package of claim 1, wherein the insulating material 59 of the first substrate layer comprises an organic material, column 8 line 14 (polyimide is organic material).

Regarding claim 6, Wu discloses the semiconductor chip package of claim 1, wherein the first conductive material comprises solder, column 8 line 12.

Regarding claim 12, Wu discloses the chip package of claim 1, wherein the stud 80 has a partially squashed boll portion 82, column 9 line 9, bonded to the chip contact pad 44, and wherein the elongated portion extends from the partially squashed ball portion 82, fig. 4.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 5130768 to Wu et al. in view of US 6833285 to Ahn et al.

Regarding claim 7, Wu does not disclose the semiconductor chip package of claim 1, wherein the first conductive material (solder) comprises a conductive adhesive.

However, Ahn discloses the solder 118 and 126 can be used interchangeably with conductive adhesive to make an electrical connection, column 9 lines 40-42. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to use the conductive adhesive teaching of Ahn to replace the solder of Wu, because such material replacement would

have been considered a mere substitution of art-recognized equivalent values, MPEP 2144.06.

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 5130768 to Wu et al. in view of US 6800947 to Sathe.

Regarding claim 8, Wu discloses the semiconductor chip package of claim 1, wherein the substrate 12 further comprises: two or more layers (150,158,159), fig. 3, having conductive trace lines 154 formed therein, a second side (where 16 is located in fig. 4) opposite the first side (where 15 is located), a terminal (154) on the second side, wherein the terminal 154 is electrically connected to the chip contact pad 44 via the stud 80, the first conductive material (solder), at least one of the conductive trace lines 154.

But, Wu does not disclose via filled with a second conductive material, wherein the terminal is electrically connected to the second conductive material in the via, and wherein the second conductive material is electrically connected to at least one of the conductive trace lines.

However, Sathe discloses a semiconductor chip package in fig. 3 wherein the IC is electrically connected to the substrate 120 comprises two or more layers 121/122/123 having conductive trace 131 formed therein; a second side (wherein 128 is located) opposite the first side (wherein 127 is located), a via 126 filled with a second conductive material (conductive via 126), wherein the terminal 128 is electrically connected to the second conductive material in the via 126, and wherein the second conductive material (conductive via 126)) is electrically connected to at least one of the conductive trace lines 131, wherein the terminal

128 is electrically connected to the chip contact pad 112/124, the first conductive material 112, at least one of the conductive trace lines 131. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the substrate teaching of Sathe to replace the substrate 12 of Wu, because it would have created a flip-chip package to decrease the weight and the thickness and to increase the flexibility of an electronics package as taught by Sathe, see abstract.

11. Claims 9-11 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5130768 to Wu et al. in view of Applicant Admitted Prior Art (APA).

Regarding claims 9-12, Wu does not disclose the semiconductor chip package of claim 1, further comprising: a support member extending from the first layer of the substrate between the chip and the substrate, wherein the chip is at least partially supported by the support member, wherein the support member comprises polymer material, and wherein the chip package further comprising an under-fill material located between the chip and the substrate.

However, APA discloses in fig 1 the semiconductor chip package comprising: a support member 30 extending from the first layer of the substrate 24 between the chip 22 and the substrate 24, wherein the chip is at least partially supported by the support member 30, wherein the support member comprises polymer material, and wherein the chip package further comprising an under-fill material located between the chip and the substrate, specification page 1 [0003].

At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the support member teaching of APA in Wu's device, because such support member is typical in the art or to distribute the stresses evenly between the chip and substrate as taught by APA, see specification pages 1-2 [0003] and [0004].

With respect to the polymer material, APA discloses the under-fill material is placed and cured, specification page 1 [0003]. It would have been obvious to one of ordinary skill in the art to understand that the curing process is normally related to polymer material, see Nagarajan (6639321) in column 4 lines 16-22.

Regarding claim 17, Wu discloses a semiconductor chip package in fig. 4 comprising: an integrated circuit chip 40, column 3 line 65, a chip contact pad 44, column 5 line 21, formed on a first side of the chip; a stud 80, column 5 line 40, formed on the chip contact pad 44, the stud 80 formed on the chip contact pad 44, the stud 80 having an elongated portion extending from the chip contact pad 44; a substrate 12, column 4 line 15, comprising a first layer 59 of insulating material, column 8 line 14, on a first side of the substrate 12, a well 15, column 8 line 14, formed in the first layer 59 (159 in fig. 3) and opening to the first side of the substrate 12, the well having a bottom, a conductive liner 56, column 8 line 15, at least partially lining the well 15, a first conductive material (solder 15), column 8 line 12, that at least partially fills the well 15, and a second layer 158, fig. 3, column 7 line 23, having conductive trace lines 154, column 7 line 18, formed therein, wherein the first conductive material (solder 15) is electrically connected to at least one of the trace lines 154, fig. 4, via the conductive

liner 56, wherein the stud 80 is partially embedded in the first conductive material (solder) to form an electrical connection between the chip 40 and the substrate 12, and wherein the first side of the chip faces the first side of the substrate, fig. 4.

But, Wu does not discloses the chip package comprises a support member extending from the first layer of the substrate between the chip and the substrate, and wherein the chip is at least partially supported by the support member.

However, APA discloses in fig 1 the semiconductor chip package comprising: a support member 30 extending from the first layer of the substrate 24 between the chip 22 and the substrate 24, wherein the chip is at least partially supported by the support member 30, specification page 1 [0003]. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the support member teaching of APA in Wu's device, because such support member is typical in the art and to distribute the stresses evenly between the chip and substrate as taught by APA, see specification pages 1-2 [0003] and [0004].

Regarding claim 18, Wu discloses the chip package of claim 17, wherein the stud 80 has a partially squashed boll portion 82, column 9 line 9, bonded to the chip contact pad 44, and wherein the elongated portion extends from the partially squashed ball portion 82, fig. 4.

Regarding claim 19, Wu discloses the semiconductor chip package of claim 1, wherein the first conductive material comprises solder, column 8 line 12.

12. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 5130768 to Wu et al. and Applicant Admitted Prior Art (APA) as applied to claims 17-19 above and further in view of US 6833285 to Ahn et al.

Regarding claim 20, Wu does not disclose the semiconductor chip package of claim 1, wherein the first conductive material (solder) comprises a conductive adhesive.

However, Ahn discloses the solder 118 and 126 can be used interchangeably with conductive adhesive to make an electrical connection, column 9 lines 40-42. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to use the conductive adhesive teaching of Ahn to replace the solder of Wu, because such material replacement would have been considered a mere substitution of art-recognized equivalent values, MPEP 2144.06.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
Patent Examiner
30 Mar. 2005